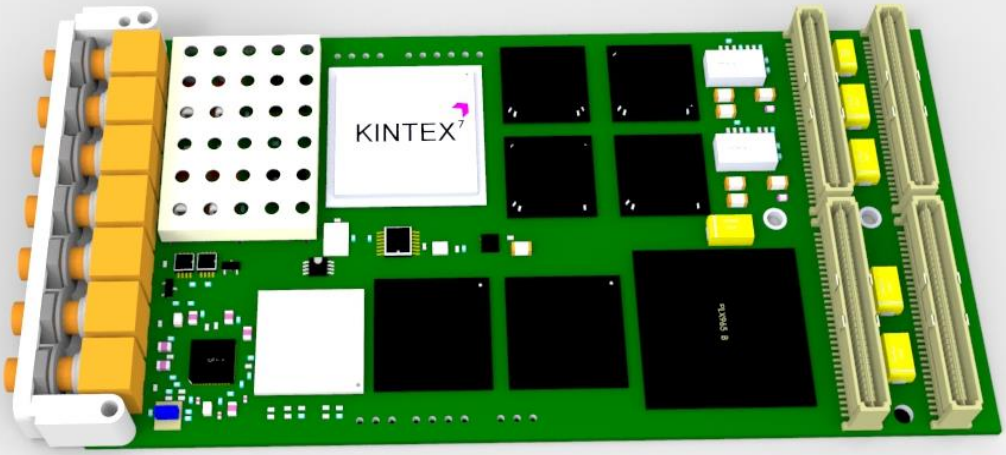
BLACKBURN SIGNAL PROCESSING



GB101: Digital Receiver PMC Module

High performance fundamentals

The GB101 is a digital receiver in PMC form factor, which will interface embedded computing systems to radio equipment at either an intermediate frequency, or at VHF radio frequencies. The card combines high performance ADCs and low jitter clock components with a Xilinx Kintex 7 FPGA and digital down converter ASICs, to produce a high performance low power digital receiver module. It will accept up to four RF/IF inputs through front panel SMA connectors and provide the host system with either digitized versions of the wide band analog input signals, or specific bands of interest down converted to baseband using the on board GC4016s ASICs. The Kintex 7 FPGA (XC7K160T) provides exceptional computational power on very reasonable power and price budgets, making the GB101 an ideal technical refresh for embedded systems built around PCI bus architectures. It will upgrade analog performance and signal processing capability of legacy systems to the state of the art, at a fraction of the cost of system replacement.

Data Conversion

The GB101 is equipped with two Texas Instruments 16DV160 dual ADCs, which digitize the analog inputs with 16 bit resolution, at rates up to 160MHz. Sample clocks for the converters can be generated on board, or an external clock can be provided from the front panel connector. The external clock may be provided at the full sample rate, or the internal clock may be phase locked to a lower frequency, such as a 10MHz system reference clock.

DDC details

The GrayChip Digital Down Converters are highly specialized digital signal processors which allow the user to extract specific channels of interest from the wideband spectrum digitized by the ADCs. Each DDC ASIC contains four discrete data processing paths, which feature a Numerically Controlled Oscillator (NCO), a mixer, CIC filter, and FIR filter. Programmable parameters of this processing chain include the NCO frequency, initial NCO phase, channel bandwidth, filter coefficients, and overall gain. When operated independently, the DDC signal processing chains provide four channels, each carrying up to 2.5MHz. The four channels of each chip may also be combined to provide two channels of 5MHz, or one channel of 10MHz bandwidth.

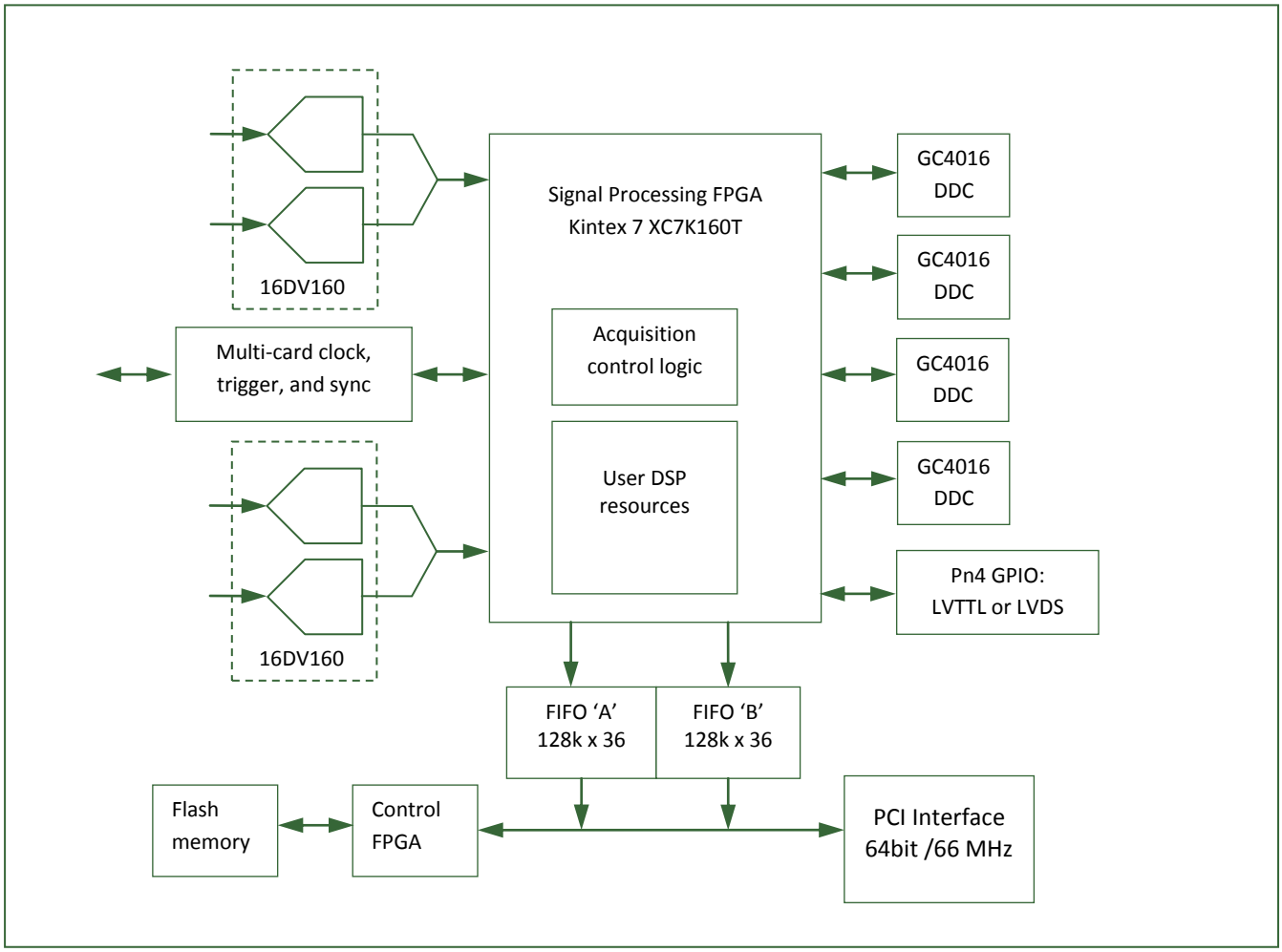
Although all narrow band outputs must be the same bandwidth, center frequencies of the individual bands may be uniquely programmed, as can the initial phase of the numerically controlled oscillator. DDCs located on multiple cards may be synchronized for phase coherent operations such as beam forming.

FPGA resources

If necessary, additional processing can be performed using the on board Kintex 7 FPGA, using the Hardware Development Kit supplied with the card. The HDK includes all VHDL source code, design documentation, and project files required for the user to continue development from the standard product configuration delivered by BBSP.

Applications information

The GB101 can be directly installed on any single board computer, or carrier card which includes a PMC site. This allows the module to be installed in a VME, cCPI, or VPX system. By using widely available carrier cards, the digital receiver capability can be installed in PCI or PCI Express slots found in desktop or industrial PCs. The dual data path memory architecture of the GB101 allows simultaneous collection of wideband and narrow band data. This is an important feature because it allows the card to support “search” and “track” modes of operation concurrently. Any of the wideband analog input data streams can be routed to one FIFO without processing, and at the same time, raw ADC data can be routed through the DDC(s) to isolate signals of interest.



GB101: 16 channel digital receiver.

Target Specifications:

Basic Architecture and Functionality

- 16 channel digital receiver in PMC form factor.
- 4 x GC4016's allow down conversion of 4 to 16 (FDM) channels from any of 4 analog inputs.
- Dual data paths allow simultaneous wideband (search) and narrow band (track) operations.
- Phase coherent operation across multiple cards guaranteed.
- Total power dissipation less than 15W.
- Open source signal processing FPGA (Xilinx Kintex 7 XC7K160T) for custom algorithm development.
- Programmable sample clock with 10MHz TCXO reference.

Analog Input Characteristics

- 2x Texas Instruments 16DV160 ADCs. 16 bit resolution at up to 160MHz
- AC coupled. Full scale input: +5.5dBm (into 50 Ohms)
- >75dB SNR with Fin 70MHz, Fs 93.333MHz.
- >82dB spur free dynamic range (SFDR)
- >70dB SINAD

Digital IO

- PLX PCI9656 PCI to local bus bridge: 64 bit 66 MHz PCI bus to 32 bit 66MHz local bus.
- 40 GPIOs routed from signal processing FPGA to Pn4 connector. Can be ordered as LVTTL and LVDS.

Integration Support

- Full Software Development Kit for Windows or Linux, with application examples written in 'C'.
- Hardware Development Kit (HDK) for on board FPGA development using Xilinx ISE or Vivado.

Environmental

- Specifications guaranteed for operation from 0 to 50 °C.
- Storage temperature -40 to +85 °C.
- Approximately 200LFM airflow required for convection cooling.
- Contact factory if conduction cooling, or extended temperature operation is required.

Who is BBSP?

The engineers who make up BBSP are sensor processing specialists. Our expertise lies in connecting sensors to computers, and processing the raw sensor data to extract signals of interest. This functionality is critical to the operation of radar, sonar, telecommunications, imaging, and test and measurement systems. Each of the members of BBSP brings over 10 years of experience interfacing the digital processing capabilities of high performance computing systems with the analog signals produced by antennae, hydrophones, accelerometers, etc. Our portfolio of past work includes products produced by Interactive Circuits and Systems, Radstone Embedded Computing, and General Electric Intelligent Platforms. Our designs ensure synchronous sampling on every channel, and robust buffering against data loss, regardless of operating system latency. And by using industry standard form factors such as PMC, XMC and VPX, our products are widely compatible with COTS equipment made by third party vendors.